20. (Amended) A transistor as recited in claim 12, [said processincluding the further step of forming] including a sidewall within said trench.

21. (Amended) A transistor as recited in claim 12, wherein said sidewall is a doped material and said [step of supplying] impurities have been supplied [is performed] by diffusion from said sidewall.

Please cancel Claim 22 without prejudice or disclaimer.

A clean copy of each amended claim appears in the attached Appendix.

REMARKS

Claims 1-21 are pending in the application. Claims 1-11 are directed to a non-elected invention and have been canceled without prejudice or disclaimer

As to the amendment to Claim 12, the lines added at the end, see, e.g., Applicants' specification at page 10, lines 28-30 and page 7, lines 4-5. As to the recitation that the impurities have a precisely desired location, see, e.g., Applicants' specification at page 10, lines 14-17. As to the recitation of the semiconductor layer being formed on an insulator layer, see Applicants' original Claim 22.

I. Anticipation Rejection Based on Kapoor

At page 2 of the Office Action, Claims 12-21 have been rejected as being anticipated by Kapoor (U.S. Patent No. 5,943,576).

Applicants respond as follows. Claim 22 has not been rejected as anticipated based on Kapoor. Above, the subject matter of Claim 22 has been

incorporated in independent Claim 12.[1] In view of the above, reconsideration and withdrawal of the anticipation rejection based on Kapoor are respectfully requested.

II. Anticipation Rejection Based on Oyamatsu

At page 3 of the Office Action, Claims 12-14, 17-19 and 20-21 have been rejected under 35 U.S.C. 102(b) as being anticipated by Oyamatsu (U.S. Patent No. 5,424,229).

Applicants respond as follows. Claim 22 has not been made the subject of this anticipation rejection, and this anticipation rejection is rendered moot by the incorporation of the subject matter of Claim 22 into independent Claim 12.

Applicants further respectfully traverse the anticipation rejection based on Oyamatsu, as follows. There is no disclosure nor suggestion in Oyamatsu that the impurities have a precisely desired location. Nor does Oyamatsu disclose an asymmetric field effect transistor that is substantially free of floating body effects.

Reconsideration and withdrawal of the anticipation rejection based on Oyamatsu are respectfully requested.

III. Obviousness Rejection Based on Kapoor or Oyamatsu, taken with Hsu (Claim 22)

At page 4 of the Office Action, Claim 22 has been rejected under 35 U.S.C. 103(a) as being unpatentable over either Kapoor or Oyamatsu, taken with Hsu (U.S. Patent No. 6,291,325). The Examiner admits that Kapoor or Oyamatsu lacks to form the transistor on a silicon on insulator (SOI) substrate. To supply this deficiency, the Examiner cites Hsu, col. 4, lines 33-46 and Figs. 10, 12, 1-3.

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[1]In amending Claim 12 above, Applicants are not admitting that the originally claimed product-by-process is the same product as the product of Kapoor. Rather, Applicants' amendment is based on problems and complexities of proof associated with the product-by-process claim format in this case.

Applicants respectfully traverse the obviousness rejection. Beyond the deficiencies of Kapoor and Oyamatsu that the Examiner admits, Kapoor and Oyamatsu are further distinguished from the presently claimed invention. Neither primary reference suggests or discloses the impurities at a precisely desired location in the respective source and drain regions. Nor does Kapoor or Oyamatsu disclose a transistor that is substantially free of floating body effects. Nor does Hsu supply these deficiencies.

A person of ordinary skill in the art, from the three cited references, would not be able to provide an asymmetrical field effect transistor, including a semiconductor on an insulator, that was substantially free of floating body effects. SOI wafers were developed for certain desired properties, but, unfortunately, in devices before the present invention, the existence of the insulator layer which supports the development of the improved quality of semiconductor material also presented a problem known in the art as floating body effect, in transistor structures.[2] The floating body effect is specific to conventional transistors formed on substrates having an insulator layer.[3] In those conventional transistors, the neutral floating body is electrically isolated by source/drain and halo extension regions that form oppositely poled diode junctions at the ends of the transistor conduction channel and floating body while the gate electrode is insulated from the conduction channel through a dielectric.[4] In the conventional transistors, the insulator layer in the substrate completes insulation of the conduction channel and thus prevents discharge of any charge that may develop in the floating body. Charge injection into the neutral body when the transistor is not conducting develops voltages in the conduction channel in accordance with the source and drain diode characteristics.[5] Such characterized the conventional SOI transistors.

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[2]Applicants' specification, page 2, lines 9-13.

[3]Id., lines 13-15.

[4]Id., lines 15-21.

[5]Id., lines 24-28.

Still referring to conventional SOI transistors, the voltage developed due to charge collection in the transistor conduction channel had the effect of altering the switching threshold, which, in turn, altered the signal timing and signal propagation speed, with the result that the diode characteristics of the source and drain in the conventional transistors had to be tailored to limit charge build-up in the floating body.[6]

At the time of the present invention, what persons of ordinary skill in the art did to tailor the diode characteristics was to make the diode junctions somewhat leaky to allow the floating body of the transistor to be discharged to an acceptable degree.[7] Unfortunately, because field effect transistors were generally formed symmetrically with identical source and drain impurity structures, development of such a characteristic reduced the ratio of resistance of the "on" and "off" states of the transistor. At the time of the present invention, there was recognized by those of ordinary skill in the art to be a trade-off between limitation of floating body effects and maintaining a suitable on-off ratio.[8] Overcoming that trade-off and providing an SOI transistor substantially free of floating body effects was beyond the contemplation of a person of ordinary skill in the art.

Before the present invention, most known designs for field effect transistors were symmetrical.[9] Thus, the Examiner's assumptions implying "asymmetry" into the cited references is not correct. A person of ordinary skill in the art would not imply "asymmetry" into an FET reference. To the contrary, most FET designs are the opposite, i.e., are symmetrical. Kapoor (patented in 1999) does not disclose an asymmetrical FET design. Oyamatsu (patented in 1995) does not disclose an asymmetrical FET.

A person of ordinary skill in the art would lack motivation to combine

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[6]Applicants' specification, paragraph bridging pages 2-3.

[7]Id., page 3, lines 8-10.

[8]Id., lines 11-23.

[9]Id., lines 24-25.

Kapoor or Oyamatsu (ordinary transistors) with a reference (such as Hsu) disclosing an asymmetrical transistor. Objectively speaking, there was nothing at the time to make such a person of ordinary skill want to modify Kapoor or Oyamatsu in that direction.

At the time of the present invention, the recognized approach to reduction of floating body effects at the then-state of the art was to form a connection from the floating body/conduction channel to the source electrode through the impurity well.[10] However, that approach was only a partial solution because the well can be highly resistive and the connection can be ineffective,[11] and did not provide an FET "substantially free of floating body effects."

Nor does Hsu, the secondary reference, mention floating body effects, or disclose or suggest an asymmetric FET that is substantially free of floating body effects. Even with the three cited references, a person of ordinary skill in the art would still not reach the presently claimed invention.

Reconsideration and withdrawal of the obviousness rejection based on Kapoor, Oyamatus and Hsu are respectfully requested.

IV. Obviousness Rejection Based on Oyamatsu with Lee (Claims 15-16)

At page 5 of the Office Action, Claims 15-16 have been rejected under 35 U.S.C. 103(a) as unpatentable over Oyamatsu taken with Lee (U.S. Patent No. 6,214,677).

The subject matter of non-rejected Claim 22 having been incorporated into base Claim 12, this obviousness rejection is believed to be removed, and no further response needed. Reconsideration and withdrawal of the obviousness rejection of Claims 15-16 are respectfully requested.

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[10]Id., lines 23-26.

[11]Id., lines 27-29.

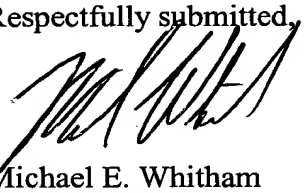
V. Obviousness Rejection Based on Oyamatsu with Chau (Claims 20-21)

At page 5 of the Office Action, Claims 20-21 have been rejected under 35 U.S.C. 103(a) as unpatentable over Oyamatsu taken with Chau (U.S. Patent No. 5,434,093).

The subject matter of non-rejected Claim 22 having been incorporated into base Claim 12, this obviousness rejection of dependent claims 20-21 is believed to be removed, and no further response needed. Reconsideration and withdrawal of this obviousness rejection of Claims 20-21 are respectfully requested.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 12-21 be allowed, and that the application be passed to issue. Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephone or personal interview. A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees to Assignee's Deposit Account No. **09-0458** (IBM/Fishkill).

Respectfully submitted,



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Appendix

Clean Copy of Amended Claims

A clean copy of amended Claims 12-21 is as follows.

12. An asymmetric field effect transistor comprising:

a trench in a dielectric layer on a semiconductor layer, said semiconductor layer including impurities supplied thereto at edges of said trench and adjacent source and drain regions, wherein the impurities have a precisely desired location, said semiconductor layer being formed on an insulator layer, and

a gate structure formed on said semiconductor layer in said trench, with asymmetrical diode properties at the source and drain regions,

wherein the transistor is substantially free of floating body effects.

13. A transistor as recited in claim 12, the dielectric layer having been removed, and comprising source and drain impurity regions formed adjacent said gate structure.

14. A transistor as recited in claim 13, said source and drain impurity regions having been formed by impurity implantation.

15. A transistor as recited in claim 13, including an insulator layer deposited over said source and drain regions and said gate structure.

16. A transistor as recited in claim 15, wherein the insulator layer is planarized to said gate structure.

17. A transistor as recited in claim 12, wherein said gate is between source and drain impurity regions.

18. A transistor as recited in claim 17, wherein said gate structure is

planarized to said dielectric layer.

19. A transistor as recited in claim 12, wherein impurities were supplied by angled implantation within said trench.

20. A transistor as recited in claim 12, including a sidewall within said trench.

21. A transistor as recited in claim 12, wherein said sidewall is a doped material and said impurities have been supplied by diffusion from said sidewall.